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1. Introduction and Summary of Test Results

Single-Event Effects (SEE) testing was previously conducted on the AMD v1200 System on Chip (SoC) at Massachusetts General Hospital's (MGH) Francis H. Burr Proton Therapy Center on May 28, 2022, using 200-MeV protons. This testing trip was purposed to verify electrical monitoring methodologies and ground support equipment compiled in the previous year, and confirm the bounds of radiation sensitivity using the baseline radiation data previously provided by Troxel Aerospace[1].

Because radiation-induced errors may have consequential effects on a system, the behavior and resiliency of software applications need to be considered in radiation environments. More so, failure of the device and an inability to reset itself should be considered detrimental to an application. This testing campaign adds to NASA Electronic Part and Packaging (NEPP) program's prior coverage on AMD Ryzen microprocessor devices.

This Proton test covered three types of test vectors: idle operation, *RAMjET*[2,3] (time-series classifier AI experiment), and *Sun or Moon*[4] (binary image classifier AI experiment). The results were aligned with expectations and show that this System on Chip is a viable candidate for space flight missions. Because the device was recoverable upon a power cycle of the computer system, its use in a radiative environment may be possible given a hardware or software watchdog routine to detect an error and reset the device according to the mitigation solutions.

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[1] Heavy Ion and Proton Test Results for Recent-Generation GPUs; Troxel et al., https://ieeexplore.ieee.org/document/9679339

[2] https://github.com/golmschenk/ramjet/tree/experimental-gpu-configuration-simplified-infer

[3] Identifying Planetary Transit Candidates in Tess Full-Frame Image Light Curves Via Convolutional Neural Networks; Olmschenk et al. (GSFC) https://ntrs.nasa.gov/citations/20210025351

[4] NEPP Processor Enclave: Testing Artificial Intelligence & Machine Learning; Wyrwas (SSAI, Inc., work performed for GSFC) https://ntrs.nasa.gov/citations/20205003132

2. Device Tested

The SoC contains the AMD Ryzen Embedded V1202b Dual Core/Quad Thread @ 2.3ghz and the AMD Radeon Vega 3 Graphics (with 3 GPU Compute-units). The SoC's power specification ranges from 17W to 30W. The test article is a single board computer (SBC) containing this SoC as a soldered down BGA much like laptop computers have. Figure 1 shows pictures of the Udoo Bolt v3 as mounted at the beam line. Table 1 gives information on this part.

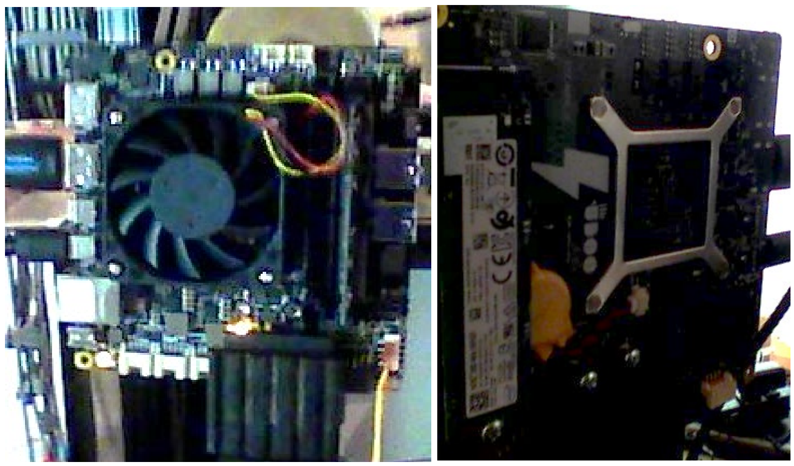

Figure 1: AMD v1200 SoC As-tested on Udoo Bolt v3

Table 1: Part Identification Information

Quantity	1
Part Model	AMD v1202
Board Model	Udoo Bolt v3
REAG ID	20-005
Manufacturer	Global Foundries
Technology	14nm LPP FF
Packaging	Flip Chip, BGA

3. Test Facility

Table 2: Test Facility Information

Facility:	Massachusetts General Hospital's (MGH) Francis H. Burr Proton Therapy Center
Ion species:	Proton
Energy:	200 MeV
Flux:	1E+08 - 1E+09 p+/sec

4. Test Setup

The DUT is a fully functional computer system. Its SoC contains the microprocessor and the GPU. A single SODIMM of 8GB DDR4 was used on the system. The operating system was Ubuntu 18.04 x64 desktop.

A. Arbiter Setup

An external arbitration computer (laptop) operating over a closed network was used to interrogate the device, execute remote commands, and monitor the DUT health. *USB over Ethernet* was used to access the test computer's mouse and keyboard. *HDMI over Ethernet* was used to view a monitor located in the operator hallway.

B. Test Vector Software

The following test payloads were performed using payload code developed at GSFC. Each one was operated with software-based sensor monitoring running on the DUT.

- Idle Operating System on the Desktop
- RAMjET
- Sun or Moon

C. Hardware Mounting

The DUT is the AMD SoC located beneath the COTS heatsink. There was sufficient clearance around the SoC, and no components were present on the secondary side of the system board within the z-axis of the chip. The beam was collimated to 1.5cm x 1.5cm. Lucite bricks were used to shield the power supply of the DUT from scattered neutrons which are a result of proton collisions within materials in the beam's path (notably its heatsink).

D. Test Procedure and Results

Five (5) runs were performed for each test configuration.

Each run resulted in pixel artifacts and a Single Event Functional Interrupt (SEFI) of the test system. It is also worth noting that upon power cycling the test system, the device behaved normally. Further, no drift in temperature was noted other than a negligible increase due to computational loading. Table 3 and Table 4 show the results of this testing campaign. It is worth noting that the flux was decreased from 1E9 to 1E8 for the final five (5) runs.

Table 3: Testing Results

Test Mode	Flux (p+/sec)	Effective Fluence (p+)	Dose rad (Si)	SEU Cross section (cm^2)	total Fluence per condition	#SEFI
IDLE	1.37E+07	9.78E+08	56.70	1.02E-09		1
IDLE	5.05E+07	5.22E+09	131.52	1.92E-10		1
IDLE	run parameters not recorded					
IDLE	1.25E+08	1.79E+09	45.21	5.58E-10		1
IDLE	1.20E+08	4.89E+09	123.30	2.04E-10		1
RAMJET	1.18E+08	8.15E+09	205.50	1.23E-10		1
RAMJET	1.21E+08	3.42E+09	86.31	2.92E-10		1
RAMJET	1.16E+08	2.93E+09	73.98	3.41E-10		1
RAMJET	1.29E+08	9.78E+09	246.60			
RAMJET	1.25E+08	2.77E+09	69.87	3.61E-10		1
SunOrMoon	1.34E+08	4.89E+09	123.30	2.04E-10		1
SunOrMoon	1.32E+08	2.93E+09	73.98	3.41E-10		1
SunOrMoon	1.34E+08	4.89E+09	123.30	2.04E-10		1
SunOrMoon	1.25E+08	1.96E+09	49.32	5.11E-10		1
SunOrMoon	1.34E+08	4.89E+09	123.30	2.04E-10	5.95E+10	1
SunOrMoon	9.35E+06	2.45E+09	61.65	4.09E-10		1
SunOrMoon	6.91E+07	2.45E+09	61.65	4.09E-10		1
SunOrMoon	5.66E+07	2.45E+09	61.65			
SunOrMoon	5.43E+07	2.45E+09	61.65	4.09E-10		1
SunOrMoon	5.80E+07	2.61E+09	65.76	3.83E-10	1.24E+10	1

Table 4: Summary of Results

	Flux (p+/sec)	Effective Fluence (p+)	SEFI Cross section (cm^2)
min	9.35E+06	9.78E+08	1.23E-10
max	1.34E+08	9.78E+09	1.02E-09
average	1.01E+08	3.93E+09	3.58E-10
standard deviation	5.26E+07	3.66E+09	3.81E-10

Acronyms

AI	Artificial Intelligence
AMD	Advanced Micro Devices
BGA	Ball Grid Array
COTS	Commercial Off the Shelf
DDR4	Dual Data Rate 4th Generation
DUT	Device Under Test
FF	FinFET (Fin Field Effect Transistor)
GPU	Graphical Processing Unit
GSFC	Goddard Space Flight Center
HDMI	High-Definition Multimedia Interface
LPP	Low Power Process
MGH	Massachusetts General Hospital
NEPP	NASA Electronic Parts and Packaging (program)
RAMjET	RApid Machine-lEarned Triage
SEE	Single Event Effects
SEFI	Single Event Functional Interrupt
SOC	System on Chip
SODIMM	Small Outline Dual Inline Memory Module
USB	Universal Serial Bus